

Main Board Card CPLD Specification

80x100GbE Switch

AS7926-80X

Version: 1.0

Revision History

Rev.	Date	Author	Revision Description
1.0	8/29/2019		Initial OCP Release

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1. CPLD overview

The ES7780BT LineCards(LC) has three CPLDs, CPLD1 for all system reset, interrupt, Control, monitor and 1588 feature. CPLD2 and CPLD3 used to decode LED information for the QSFP28/SFP+ ports control monitor it and light system LED.

I2C address info:

- *CPLD1:0x60 for CPU and BMC I2C interface
- *CPLD2:0x62 for CPU I2C interface
- *CPLD3:0x63 for CPU I2C interface

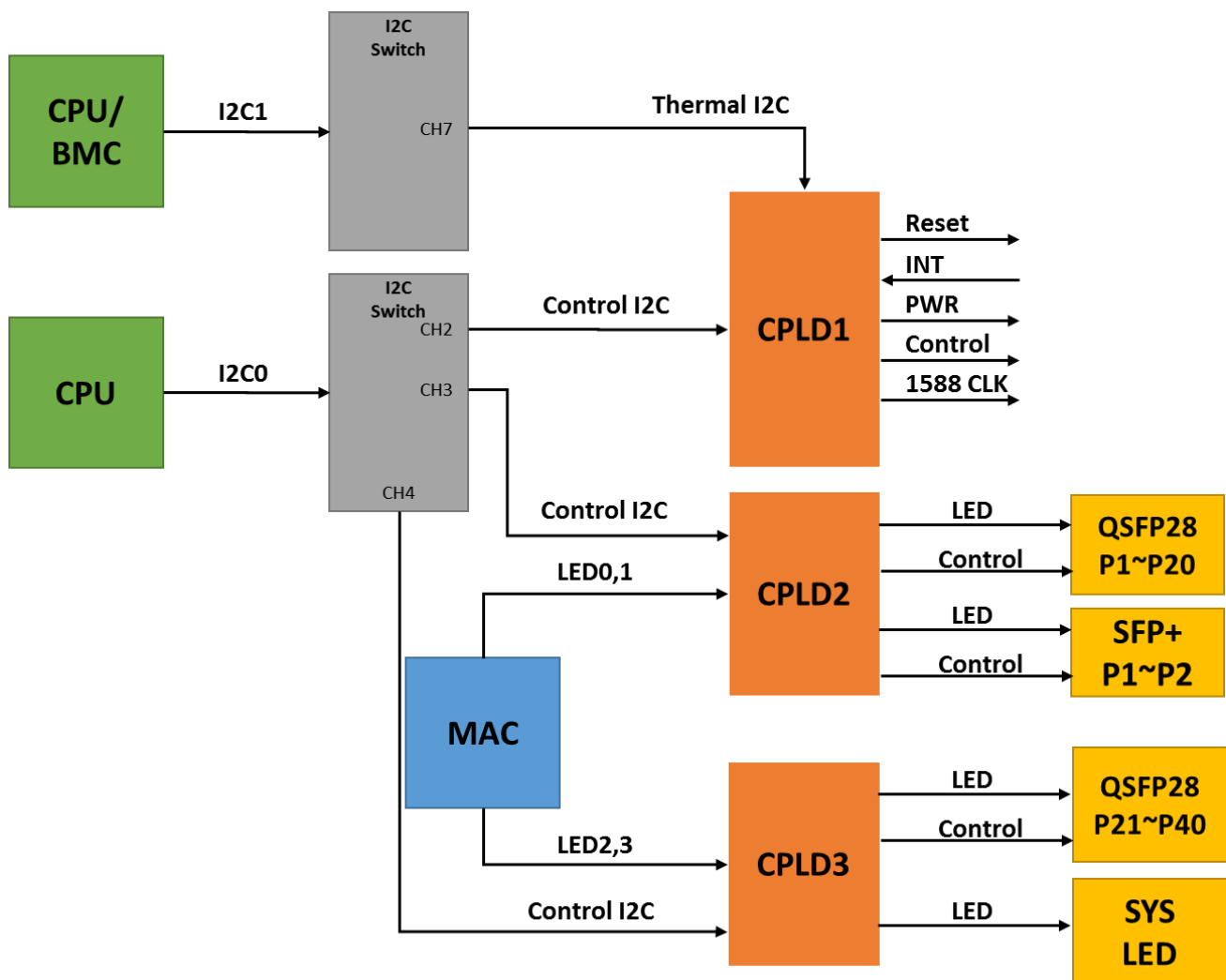


Figure 1-1 CPLD Architecture for Line Card

1.1. CPLD 1 Architecture

Reset

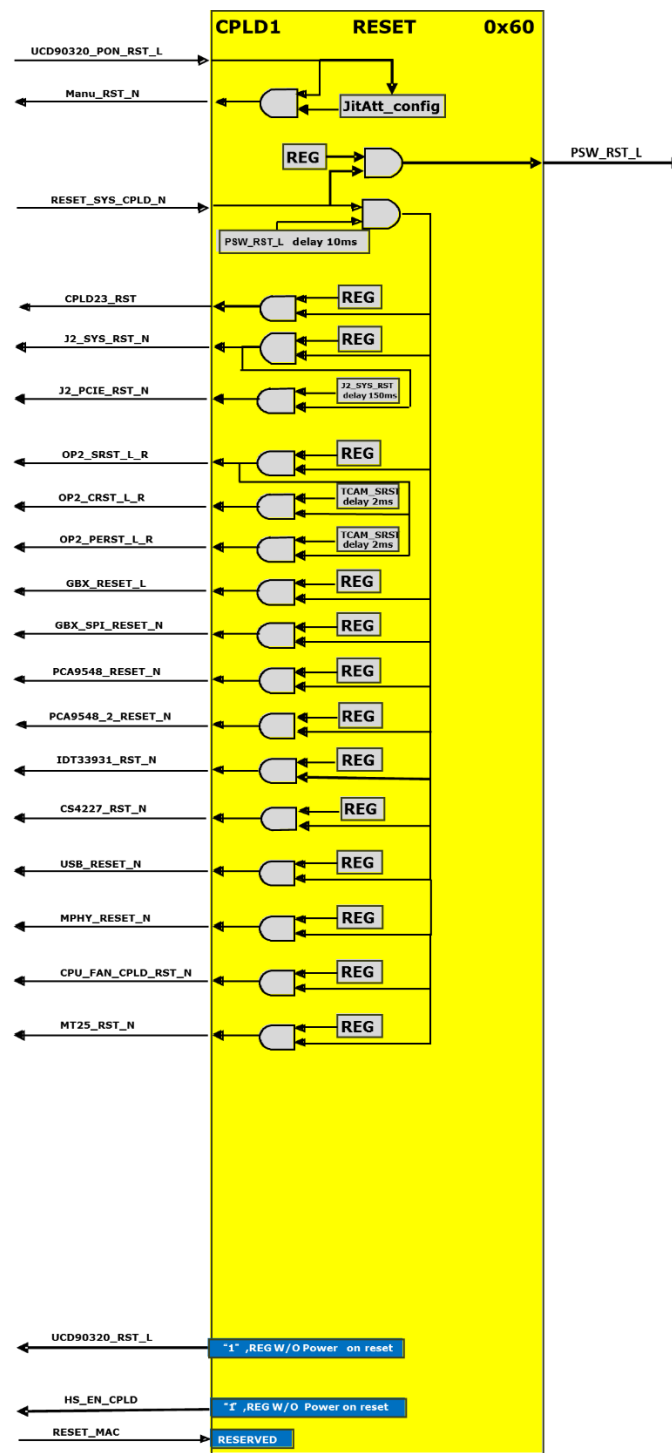


Figure 1-2 Reset Block Diagram

The reset source is from “UCD90320_PON_RST_L”, then CPLD need to config the Jitter Attenuator via I2C or SPI interface. After Jitter Attenuator be configed, reset will be passed via “MANU_RST” to the CPU modules. When CPU module is ready, they will pass “RESET_SYS_CPLD” to CPLD1 and reset all devices.

To make PCI-E topology worked, all PCI-E devices need to wait PCI-E switch ready before they can release the reset. Therefore, CPLD need to release the “PSW_RST_L” at the same time after CPU release “RESET_SYS_CPLD” and wait 10ms to release other devices. There also have registers can use to reset individual chips.

For Jericho2 and OP2, Broadcom has reset sequence requirement to initial the devise. For Jericho2, “J2_SYS_RST_N” need to be released first then wait 150ms to release “J2_PCIE_RST_N”. For OP2, “SRST” need to be released first then wait 2ms to release “CRST” and “PERST”.

“UCD90320_RST_L” and “HS_EN_CPLD” need to be set to “high” as default value without power on reset. Reset MAC is a reserved input which used to reset MAC only.

I2C access

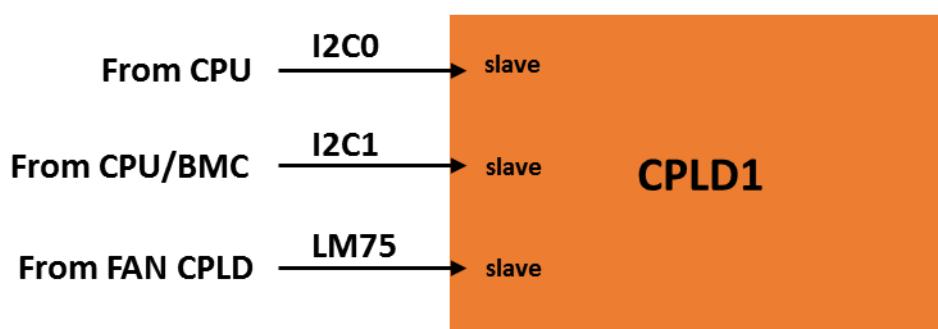


Figure 1-3 I2C Access Block Diagram

Interrupt

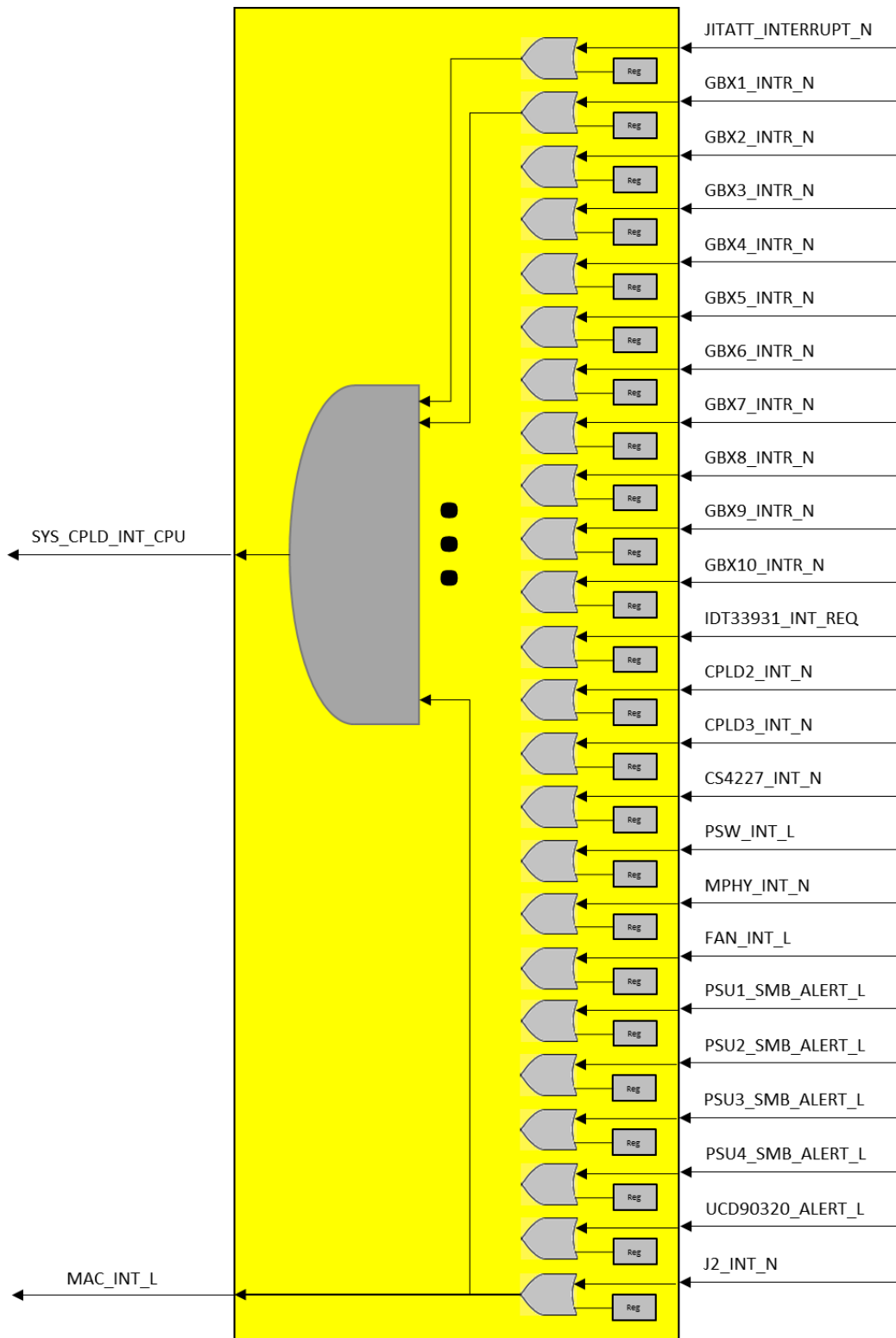


Figure 1-4 Interrupt Block Diagram

If an interrupt occurs, CPLD1 informs CPU Module by “SYS_CPLD_INT_CPU”, CPLD2&3 inform the appropriate CPU via CPLD1. Register will record the interrupt status.

Mask register blocks the interrupt to CPU.

Clock

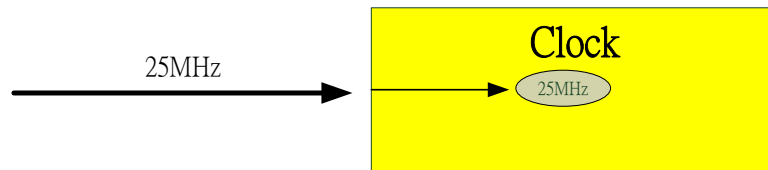


Figure 1-5 Clock Block Diagram

The CPLD reference clock is 25MHz. The 125MHz is used for the I2C transfers at 100KHz.

1.2. CPLD 2 Architecture

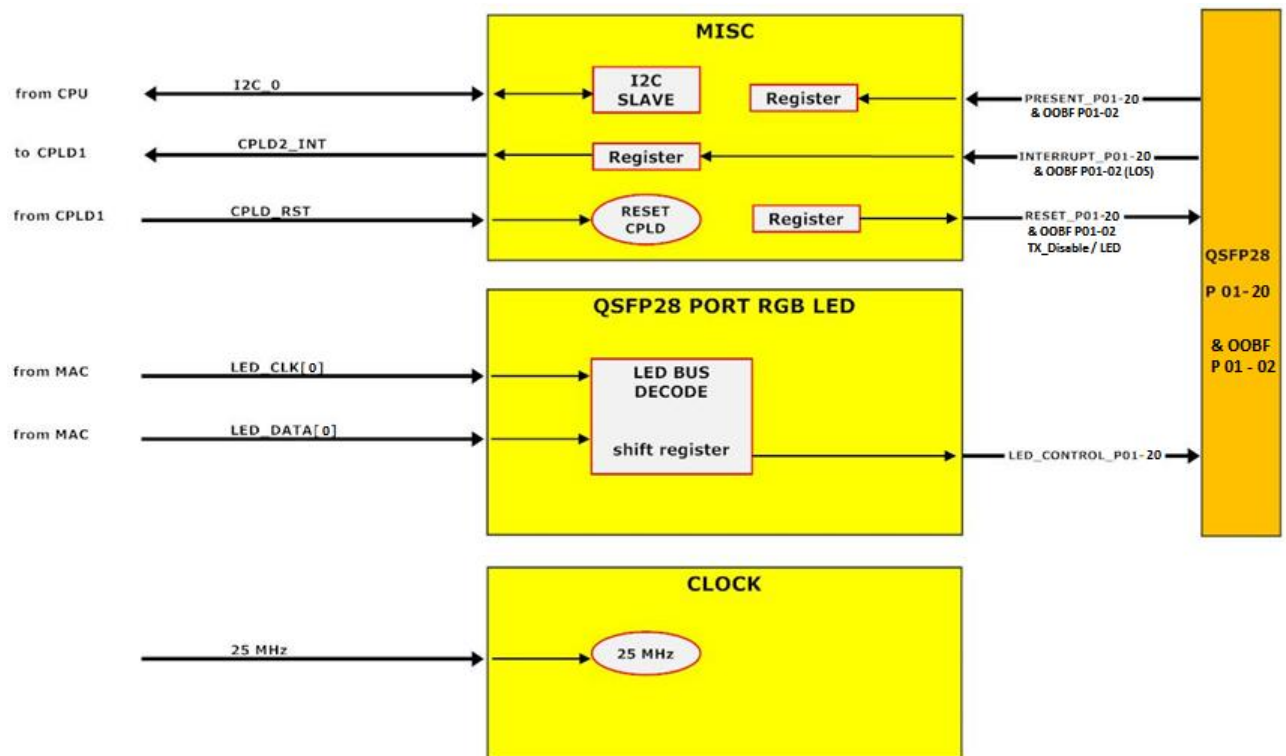


Figure 1-6 CLPD2 Block Diagram

The Front RGB LED for the QSFP28 connectors show different LED color when the port link on 40G/ 2x50G/ 100G speed.

I2C_0 is the CPLD control bus. From I2C_0, CPU can read/ write CPLD internal register.
CPLD_RST will rest the CPLD2 to default value

Port	00	01	02	03	04	05	06	07
PM	0	0	0	0	1	1	1	1
SDR NO.	00:01	02:03	04:05	06:07	08:09	10:11	12:13	14:15

→→

Output Order→→→→→→→→→→→→→→→→→→→→→→→→→→→→→

Port x	Speed (LED0)			Link/Act (LED1)		
Bit	1	2	3	4	5	6
Color	R	G	B	R	G	B

1.3. CPLD 3 Architecture

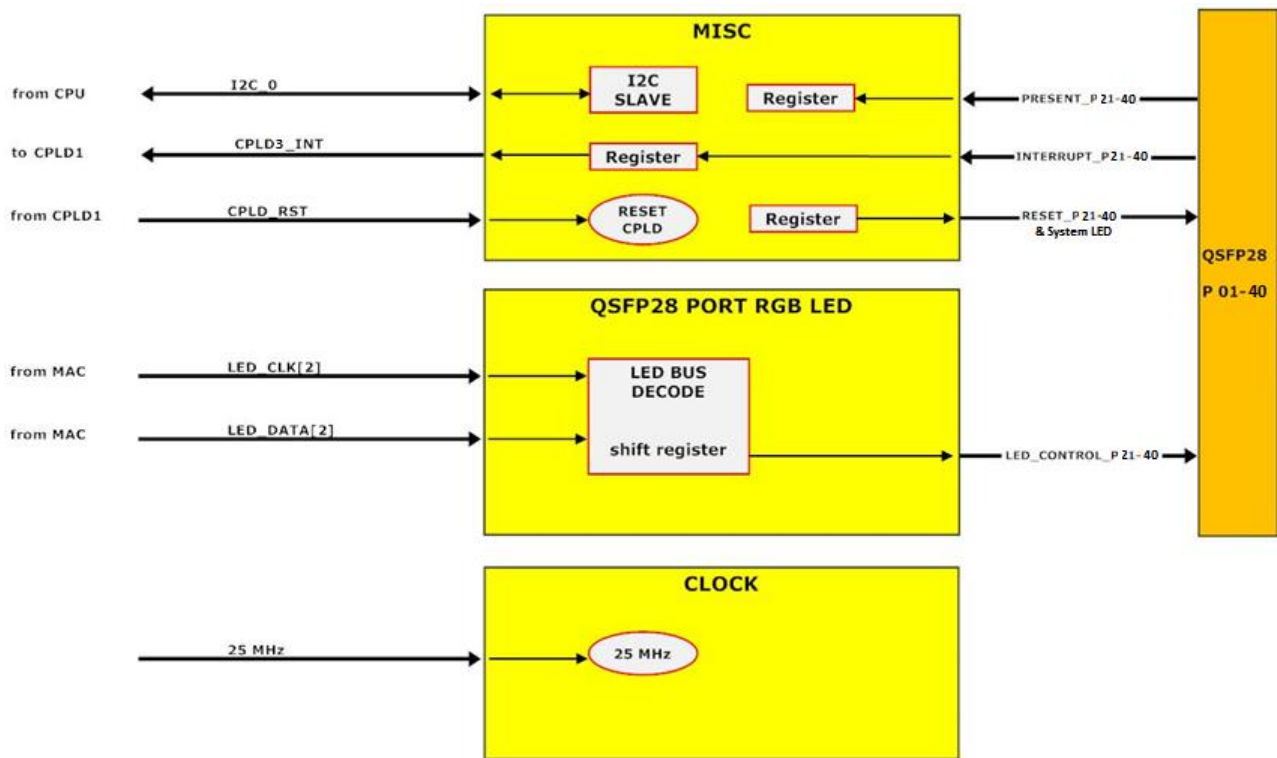


Figure 1-7 CLPD3 Block Diagram

The Front RGB LED for the QSFP28 connectors show different LED color when the port link on 4x10G/ 40G/ 4x25G/ 100G speed.

I2C_0 is the CPLD control bus. From I2C_0, CPU can read/ write CPLD internal register.
CPLD_RST will rest the CPLD2 to default value

Port	20	21	22	23	24	25	26	27
PM	5	5	5	5	11	11	11	11
SDR NO.	40:41	42:43	44:45	46:47	88:89	90:91	92:93	94:95

Port	28	29	30	31	32	33	34	35
PM	10	10	10	10	9	9	9	9
SDR NO.	80:81	82:83	84:85	86:87	72:73	74:75	76:77	78:79

Port	36	37	38	39
PM	8	8	8	8
SDR NO.	64:65	66:67	68:69	70:71

Port x	Speed (LED0)			Link/Act (LED1)		
Bit	1	2	3	4	5	6
Color	R	G	B	R	G	B

Address CPU	Register	R/W	Default value
0x00	Board Info	Read Only	
0x01	CPLD version	Read Only	
0x03	REMOTE ACCESS	Read & Write	
0x08	System Reset-1	Read & Write	0xFF
0x09	System Reset-2	Read & Write	0xFF
0x0A	System Reset-3	Read & Write	0xFF
0x10	Interrupt Status-1	Read Only	
0x11	Interrupt Status-2	Read Only	
0x12	Interrupt Status-3	Read Only	

0x13	Interrupt Status-4	Read Only	
0x20	Interrupt Mask-1	Read & Write	0x00
0x21	Interrupt Mask-2	Read & Write	0x00
0x22	Interrupt Mask-3	Read & Write	0x00
0x23	Interrupt Mask-4	Read & Write	0x00
0x30	CPU thermal value	Read & Write	0x7F
0x31	MAC thermal value	Read & Write	0x7F
0x40	Recovery Clock Valid	Read Only	
0x41	Recovery Clock Select	Read & Write	0x00
0x50	Power Supply Control	Read & Write	0x00
0x51	Power Supply Status-1	Read Only	
0x52	Power Supply Status-2	Read Only	
0x53	Power Supply Status-3	Read Only	
0x60	MISC-1	Read & Write	0x01
0x61	MISC-2	Read & Write	0x01

1.4.1. Offset 0x00 Board Info (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved	NA	NA	
3:2	PCB_ID[1:0]	R	NA	00: ASF7680 Bottom board 01: ASF7680 Top board 10: Reserved 11: Reserved
1:0	PCB_version[1:0]	R	NA	00: R0A 01: R0B 10: R01 Others: Reserved

1.4.2. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x00	CPLD version

1.4.3. Offset 0x03 Remote Access (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	HS_PWRGD	R	1	1: Hotswap 12VDC to LC above valid minimum 0: Hotswap 12VDC to LC below valid minimum
6	HS_FAULT_N	R	1	1: Normal Operataion 0: Fault
5:3	Reserve	NA	NA	
2	Hotswap_EN_CPLD	R/W	1 (W/O power on reset)	1: HotSwap can power 12VDC to LC 0: HotSwap circuit prevented from 12VDC to LC
1	Reserve	NA	NA	
0	UCD90320_RST_L	R/W	1 (W/O power on reset)	1: Release Software reset of power monitor 0: Software reset the power monitor

1.4.4. Offset 0x08 System Reset-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reset* Jericho2	R/W	1	1: J2_SYS_RST_N is placed in normal operation state. 0: J2_SYS_RST_N is placed in reset state.
6	Reset* Manu_RST	R/W	1	1: Manu_RST_N is placed in normal operation state. 0: Manu_RST_N is placed in reset state.
5	Reset* OP2	R/W	1	1: OP2_SRST_L_R is placed in operation state. 0: OP2_SRST_L_R is placed in reset state.
4	Reset* Gearbox	R/W	1	1: GBX_RESET_L is placed in operation state. 0: GBX_RESET_L is placed in reset state.
3	Reset* PCI-E Switch	R/W	1	1: PSW_RST_L switch is placed in normal operation state. 0: PSW_RST_L switch is placed in reset state.
2	Reset* CPLD2 and CPLD3	R/W	1	1: CPLD23_RST is placed in normal operation state. 0: CPLD23_RST is placed in reset state
1	Reset* Gearbox SPI EEPROM	R/W	1	1: GBX_SPI_RESET is placed in normal operation state. 0: GBX_SPI_RESET is placed in reset state.
0	Reset* J2 QSPI Flash	R/W	1	1: MT25_RST_N is placed in normal operation state. 0: MT25_RST_N is placed in reset state.

1.4.5. Offset 0x09 System Reset-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:5	Reserve	NA	NA	
4	RESET_MAC	R/W	1	Reserve
3	Reset* MGMT PHY	R/W	1	1: MPHY_RESET_N is placed in normal operation state. 0: MPHY_RESET_N is placed in reset state.
2	Reset* USB	R/W	1	1: USB_RESET_N is placed in normal operation state. 0: USB_RESET_N is placed in reset state.
1	Reset* CS4227	R/W	0 Need to release by user after system boot up	1: CS4227_RST_N is placed in normal operation state. 0: CS4227_RST_N is placed in reset state.
0	Reset* WANPLL	R/W	1	1: IDT33931_RST_N is placed in normal operation state. 0: IDT33931_RST_N is placed in reset state.

1.4.6. Offset 0x0A System Reset-7 CPU A/B (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reset* FAN CPLD	R/W	1	1: CPU_FAN_CPLD_RST_N is placed in normal operation state. 0: CPU_FAN_CPLD_RST_N is placed in reset state.
6	Reserve	NA	NA	
5	Reserve	NA	NA	
4	Reserve	NA	NA	
3	Reserve	NA	NA	
2	Reset* PCA9548_RESET_N (I2C_1; 0x75)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
1	Reset* PCA9548_2_RESET_N (I2C_0; 0x75)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
0	Reserve	NA	NA	

1.4.7. Offset 0x10 Interrupt Status-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	INTB*Jitter Attenuator	R	NA	1:No interrupt 0: There is INTR from JITATT_INTERRUPT_N
6	INTB* WAN PLL	R	NA	1:No interrupt 0: There is INTR from IDT33931_INT_REQ
5	INTB*CPLD 2	R	NA	1:No interrupt 0: There is INTR from CPLD2_INT_N
4	INTB*CPLD 3	R	NA	1: No interrupt 0: There is INTR from this CPLD3_INT_N
3	INTB*CS4227	R	NA	1: No interrupt 0: There is INTR from CS4227_INT_N
2	INTB*PCI-E Switch	R	NA	1: No interrupt 0: There is INTR from PSW_INT_L
1	INTB*MGMT PHY	R	NA	1: No interrupt 0: There is INTR from MPHY_INT_N
0	INTB*MAC	R	NA	1: No interrupt 0: There is INTR from J2_INT_N

1.4.8. Offset 0x11 Interrupt Status-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	INTB*Gearbox 1	R	NA	1:No interrupt 0: There is INTR from GBX1_INTR_N
6	INTB*Gearbox 2	R	NA	1:No interrupt 0: There is INTR from GBX2_INTR_N
5	INTB*Gearbox 3	R	NA	1: No interrupt 0: There is INTR from GBX3_INTR_N
4	INTB*Gearbox 4	R	NA	1: No interrupt 0: There is INTR from GBX4_INTR_N
3	INTB*Gearbox 5	R	NA	1: No interrupt 0: There is INTR from GBX5_INTR_N
2	INTB*Gearbox 6	R	NA	1: No interrupt 0: There is INTR from GBX6_INTR_N

1	INTB*Gearbox 7	R	NA	1: No interrupt 0: There is INTR from GBX7_INTR_N
0	INTB*Gearbox 8	R	NA	1: No interrupt 0: There is INTR from GBX8_INTR_N

1.4.9. Offset 0x12 Interrupt Status-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	INTB*Gearbox 9	R	NA	1:No interrupt 0: There is INTR from GBX9_INTR_N
6	INTB*Gearbox 10	R	NA	1:No interrupt 0: There is INTR from GBX10_INTR_N
5	INTB*Power Monitor Alarm	R	NA	1:No interrupt 0: There is INTR from UCD90320_ALERT_L
4	Reserve	NA	NA	
3	Reserve	NA	NA	
2	Reserve	NA	NA	
1	Reserve	NA	NA	
0	Reserve	NA	NA	

1.4.10. Offset 0x13 Interrupt Status-4 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA	NA	
6	Reserve	NA	NA	
5	Reserve	NA	NA	
4	INTB*Fan Board	R	NA	1: No interrupt 0: There is INTR from FAN_INT_L
3	INTB*PSU1 SMB Alarm	R	NA	1: No interrupt 0: There is INTR from PSU1_SMB_ALERT_L
2	INTB*PSU2 SMB Alarm	R	NA	1: No interrupt 0: There is INTR from PSU2_SMB_ALERT_L
1	INTB*PSU3 SMB Alarm	R	NA	1: No interrupt 0: There is INTR from PSU3_SMB_ALERT_L
0	INTB*PSU4 SMB Alarm	R	NA	1: No interrupt

				0: There is INTR from PSU4_SMB_ALERT_L
--	--	--	--	--

1.4.11. Offset 0x20 Interrupt Mask-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	INTM*Jitter Attenuator	R/W	0	1:Mask the interrupt from JITATT_INTERRUPT_N 0: Disable the Mask
6	INTM* WAN PLL	R/W	0	1:Mask the interrupt from IDT33931_INT_REQ 0: Disable the Mask
5	INTM*CPLD 2	R/W	0	1:Mask the interrupt from CPLD2_INT_N 0: Disable the Mask
4	INTM*CPLD 3	R/W	0	1: Mask the interrupt from this CPLD3_INT_N 0: Disable the Mask
3	INTM*CS4227	R/W	0	1: Mask the interrupt from CS4227_INT_N 0: Disable the Mask
2	INTM*PCI-E Switch	R/W	0	1: Mask the interrupt from INTR PSW_INT_L 0: Disable the Mask
1	INTM*MGMT PHY	R/W	0	1: Mask the interrupt from INTR MPHY_INT_N 0: Disable the Mask
0	INTM*MAC	R/W	0	1: Mask the interrupt from INTR from J2_INT_N 0: Disable the Mask

1.4.12. Offset 0x21 Interrupt Mask-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	INTM*Gearbox 1	R/W	0	1:Mask the interrupt from GBX1_INTR_N 0: Disable the Mask
6	INTM*Gearbox 2	R/W	0	1:Mask the interrupt from GBX2_INTR_N 0: Disable the Mask
5	INTM*Gearbox 3	R/W	0	1: Mask the interrupt from GBX3_INTR_N 0: Disable the Mask
4	INTM*Gearbox 4	R/W	0	1: Mask the interrupt from GBX4_INTR_N 0: Disable the Mask
3	INTM*Gearbox 5	R/W	0	1: Mask the interrupt from GBX5_INTR_N 0: Disable the Mask

2	INTM*Gearbox 6	R/W	0	1: Mask the interrupt from GBX6_INTR_N 0: Disable the Mask
1	INTM*Gearbox 7	R/W	0	1: Mask the interrupt from GBX7_INTR_N 0: Disable the Mask
0	INTM*Gearbox 8	R/W	0	1: Mask the interrupt from GBX8_INTR_N 0: Disable the Mask

1.4.13. Offset 0x22 Interrupt Mask-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	INTM*Gearbox 9	R/W	0	1:Mask the interrupt from GBX9_INTR_N 0: Disable the Mask
6	INTM*Gearbox 10	R/W	0	1:Mask the interrupt from GBX10_INTR_N 0: Disable the Mask
5	INTM*Power Monitor Alarm	R/W	0	1: Mask the interrupt from UCD90320_ALERT_L 0: Disable the Mask
4	Reserve	NA	NA	
3	Reserve	NA	NA	
2	Reserve	NA	NA	
1	Reserve	NA	NA	
0	Reserve	NA	NA	

1.4.14. Offset 0x23 Interrupt Mask-4 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	NA	NA	
6	Reserve	NA	NA	
5	Reserve	NA	NA	
4	INTM*Fan Board	R/W	0	1: Mask the interrupt from FAN_INT_L 0: Disable the Mask
3	INTM*PSU1 SMB Alarm	R/W	0	1: Mask the interrupt from PSU1_SMB_ALERT_L 0: Disable the Mask
2	INTM*PSU2 SMB Alarm	R/W	0	1: Mask the interrupt from PSU2_SMB_ALERT_L 0: Disable the Mask
1	INTM*PSU3 SMB Alarm	R/W	0	1: Mask the interrupt from PSU3_SMB_ALERT_L

				0: Disable the Mask
0	INTM*PSU4 SMB Alarm	R/W	0	1: Mask the interrupt from PSU4_SMB_ALERT_L 0: Disable the Mask

1.4.15. 0x30 CPU thermal value (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	CPU thermal value	I2C0 R/W LM75 R	0x7F	Thermal value of CPU with 2's complement integer. CPU needs to put its own thermal value in to this register. LM75 can only read value from this register

1.4.16. 0x31 MAC thermal value (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:0	MAC thermal value	I2C0 R/W LM75 R	0x7F	Thermal value of MAC with 2's complement integer. CPU needs to put thermal value of MAC in to this register. LM75 can only read value from this register

1.4.17. Offset 0x40 Recovery Clock Valid (Read Only)

Bit	Name	R/W	Reset Value	Description
7	CLK_SEL_4K	R/W	0	1: 4KHz clock comes from CPLD 0: 4KHz clock comes from WANPLL
6	Reserve	NA	NA	
5	Jitter Attenuator LOCK	R	NA	1: JITATT_LOCK is VALID 0: JITATT_LOCK is not VALID
4	WANPLL DPLL3 LOCK	R	NA	1: IDT33931_DPLL3_LOCK is VALID 0: IDT33931_DPLL3_LOCK is not VALID
3	WANPLL DPLL2 LOCK	R	NA	1: IDT33931_DPLL2_LOCK is VALID 0: IDT33931_DPLL2_LOCK is not VALID
2	WANPLL DPLL1 LOCK	R	NA	1: IDT33931_DPLL1_LOCK is VALID 0: IDT33931_DPLL1_LOCK is not VALID
1	J2_SYNCE_1_CLK_OUT_VALID	R	NA	1: J2_SYNCE_1_CLK_OUT_VALID is VALID

				0: J2_SYNCE_1_CLK_OUT_VALID is not VALID
0	J2_SYNCE_0_CLK_OUT_VALID	R	NA	1: J2_SYNCE_0_CLK_OUT_VALID is VALID 0: J2_SYNCE_0_CLK_OUT_VALID is not VALID

1.4.18. Offset 0x41 Recovery Clock Select (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	GBX_RCLK_PRI_SEL[3:0]	R/W	0	Select primary recovery clock source from which Gearbox 0000: Gearbox1 0001: Gearbox2 0010: Gearbox3 0011: Gearbox4 0100: Gearbox5 0101: Gearbox6 0110: Gearbox7 0111: Gearbox8 1000: Gearbox9 1001: Gearbox10 1010~1111: Reserve
3:0	GBX_RCLK_SEC_SEL[3:0]	R/W	0	Select Secondary recovery clock source from which Gearbox 0000: Gearbox1 0001: Gearbox2 0010: Gearbox3 0011: Gearbox4 0100: Gearbox5 0101: Gearbox6 0110: Gearbox7 0111: Gearbox8 1000: Gearbox9 1001: Gearbox10 1010~1111: Reserve

1.4.19. Offset 0x50 Power Supply Control (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	PSU3_PSON_L	R/W	0	1: Disabled output of Power Supply 3 0: Enabled output of Power Supply 3
2	PSU2_PSON_L	R/W	0	1: Disabled output of Power Supply 2 0: Enabled output of Power Supply 2
1	PSU1_PSON_L	R/W	0	1: Disabled output of Power Supply 1 0: Enabled output of Power Supply 1
0	PSU0_PSON_L	R/W	0	1: Disabled output of Power Supply 0 0: Enabled output of Power Supply 0

1.4.20. Offset 0x51 Power Supply Status-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	UPPER_FAN_HS_PGD	R	NA	1: Upper Fan board power is ok 0: Upper Fan board power is not ok
6	LOWER_FAN_HS_PGD	R	NA	1: Lower Fan board power is ok 0: Lower Fan board power is not ok
5	Reserve	NA	NA	
4	Reserve	NA	NA	
3	PSU3_PRESENT_L	R	NA	1: Power Supply 3 is not present 0: Power Supply 3 is present
2	PSU2_PRESENT_L	R	NA	1: Power Supply 2 is not present 0: Power Supply 2 is present
1	PSU1_PRESENT_L	R	NA	1: Power Supply 1 is not present 0: Power Supply 1 is present
0	PSU0_PRESENT_L	R	NA	1: Power Supply 0 is not present 0: Power Supply 0 is present

1.4.21. Offset 0x52 Power Supply Status-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	PSU3_ACOK_H	R	NA	1: Power Supply 3 AC input is ok

				0: Power Supply 3 AC input is not ok
6	PSU2_ACOK_H	R	NA	1: Power Supply 2 AC input is ok 0: Power Supply 2 AC input is not ok
5	PSU1_ACOK_H	R	NA	1: Power Supply 1 AC input is ok 0: Power Supply 1 AC input is not ok
4	PSU0_ACOK_H	R	NA	1: Power Supply 0 AC input is ok 0: Power Supply 0 AC input is not ok
3	PSU3_PWOK_H	R	NA	1: Power Supply 3 DC output is ok 0: Power Supply 3 DC output is not ok
2	PSU2_PWOK_H	R	NA	1: Power Supply 2 DC output is ok 0: Power Supply 2 DC output is not ok
1	PSU1_PWOK_H	R	NA	1: Power Supply 1 DC output is ok 0: Power Supply 1 DC output is not ok
0	PSU0_PWOK_H	R	NA	1: Power Supply 0 DC output is ok 0: Power Supply 0 DC output is not ok

1.4.22. Offset 0x52 Power Supply Status-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	Reserve	NA	NA	
2:0	J2_ROV[2:0]	R	NA	J2 ROV value 000: 0.87V (initial state) 001: 0.87V (Typical) 010: 0.81V TBD: TBD

1.4.23. Offset 0x60 MISC-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3:0	CS4227_EEPROM[4:1]	R/W	0001	CS4227 EEPROM Selest. Need to reset CS4227 after the value changed to make the setting work. 0001: Optic Transceiver for OOB 1 & 2 0010: Optic Transceiver for OOB 1 and DAC for OOB 2

				0100: DAC for OOBF 1 and Optic Transceiver for OOBF2 1000: DAC for OOBF 1 &2 Other Value: Do not use.
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1.4.24. Offset 0x61 MISC-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
4:7	Reserve	NA	NA	
1	SW1_SELECT Bottom Main Board Only	R/W	0	1: Switch the JTAG to Top Main Board chain 0: Switch the JTAG to Bottom Main Board chain
0	EE_WP	R/W	1	1: Enable write protect of MFG EEPROM 0: Disable write protect of MFG EEPROM

1.5. Line Card CPLD2 Register

Table 1-2 CPLD2 I/O Register Table

Address CPU	Register	R/W	Default value
0x01	CPLD version	Read Only	
0x08	QSFP Transceiver Reset-1	Read & Write	0xFF
0x09	QSFP Transceiver Reset-2	Read & Write	0xFF
0x0A	QSFP Transceiver Reset-3	Read & Write	0xFF
0x0B	OOBF SFP Transceiver TX-Disable	Read & Write	0xFF
0x10	QSFP Transceiver Present-1	Read Only	
0x11	QSFP Transceiver Present-2	Read Only	
0x12	QSFP Transceiver Present-3	Read Only	
0x13	OOBF SFP Transceiver Present	Read Only	
0x20	QSFP Transceiver Interrupt-1	Read Only	
0x21	QSFP Transceiver Interrupt-2	Read Only	
0x22	QSFP Transceiver Interrupt-3	Read Only	
0x23	OOBF SFP Transceiver LoS	Read Only	
0x30	OOBF SFP Transceiver LED	Read & Write	0xFF

1.5.1. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x00	CPLD version

1.5.2. Offset 0x08 QSFP Transceiver Reset-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	QSFP_RST_N_P08	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
6	QSFP_RST_N_P07	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
5	QSFP_RST_N_P06	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
4	QSFP_RST_N_P05	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
3	QSFP_RST_N_P04	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
2	QSFP_RST_N_P03	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
1	QSFP_RST_N_P02	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
0	QSFP_RST_N_P01	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

1.5.3. Offset 0x09 QSFP Transceiver Reset-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	QSFP_RST_N_P16	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
6	QSFP_RST_N_P15	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
5	QSFP_RST_N_P14	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
4	QSFP_RST_N_P13	R/W	1	1: Disable QSFP Transceiver Reset

				0: Enable QSFP Transceiver Reset
3	QSFP_RST_N_P12	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
2	QSFP_RST_N_P11	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
1	QSFP_RST_N_P10	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
0	QSFP_RST_N_P09	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

1.5.4. Offset 0x0A QSFP Transceiver Reset-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	QSFP_RST_N_P20	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
2	QSFP_RST_N_P19	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
1	QSFP_RST_N_P18	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
0	QSFP_RST_N_P17	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

1.5.5. Offset 0x0B OOB SFP Transceiver TX-Disable (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:2	Reserve	NA	NA	
1	TX_DIS_FX1	R/W	1	1: Disable OOB SFP Transmitter 0: Enable OOB SFP Transmitter
0	TX_DIS_FX0	R/W	1	1: Disable OOB SFP Transmitter 0: Enable OOB SFP Transmitter

1.5.6. Offset 0x10 QSFP Transceiver Present-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_PRSNT_P08	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
6	QSFP_PRSNT_P07	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
5	QSFP_PRSNT_P06	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
4	QSFP_PRSNT_P05	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
3	QSFP_PRSNT_P04	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
2	QSFP_PRSNT_P03	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
1	QSFP_PRSNT_P02	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
0	QSFP_PRSNT_P01	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1.5.7. Offset 0x11 QSFP Transceiver Present-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_PRSNT_P16	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
6	QSFP_PRSNT_P15	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
5	QSFP_PRSNT_P14	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
4	QSFP_PRSNT_P13	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
3	QSFP_PRSNT_P12	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
2	QSFP_PRSNT_P11	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1	QSFP_PRSENT_P10	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
0	QSFP_PRSENT_P09	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1.5.8. Offset 0x12 QSFP Transceiver Present-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	QSFP_PRSENT_P20	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
2	QSFP_PRSENT_P19	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
1	QSFP_PRSENT_P18	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
0	QSFP_PRSENT_P17	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1.5.9. Offset 0x13 OOB SFP Transceiver Present (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	Reserve	NA	NA	
1	PRESENT_FX1	R	NA	1: OOB SFP Transceiver did not present 0: OOB SFP Transceiver is present
0	PRESENT_FX0	R	NA	1: OOB SFP Transceiver did not present 0: OOB SFP Transceiver is present

1.5.10. Offset 0x20 QSFP Transceiver Interrupt-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_INT_P08	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
6	QSFP_INT_P07	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
5	QSFP_INT_P06	R	NA	1: QSFP Transceiver Interrupt de-assert

				0: QSFP Transceiver Interrupt assert
4	QSFP_INT_P05	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
3	QSFP_INT_P04	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
2	QSFP_INT_P03	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
1	QSFP_INT_P02	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
0	QSFP_INT_P01	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert

1.5.11. Offset 0x21 QSFP Transceiver Interrupt-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_INT_P16	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
6	QSFP_INT_P15	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
5	QSFP_INT_P14	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
4	QSFP_INT_P13	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
3	QSFP_INT_P12	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
2	QSFP_INT_P11	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
1	QSFP_INT_P10	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
0	QSFP_INT_P09	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert

1.5.12. Offset 0x22 QSFP Transceiver Interrupt-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
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7:4	Reserve	NA	NA	
3	QSFP_INT_P20	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
2	QSFP_INT_P19	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
1	QSFP_INT_P18	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
0	QSFP_INT_P17	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert

1.5.13. Offset 0x23 OOB SFP Transceiver LoS (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	Reserve	NA	NA	
1	RX_LOSS_FX1	R	NA	1: OOB SFP Transceiver LoS assert 0: OOB SFP Transceiver LoS de-assert
0	RX_LOSS_FX0	R	NA	1: OOB SFP Transceiver LoS assert 0: OOB SFP Transceiver LoS de-assert

1.5.14. Offset 0x30 OOB SFP Transceiver LED (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	SFP2_LED_ERR_N	R/W	1	1: Off LED / LED Control by CS4227 0: Light LED
2	SFP1_LED_ERR_N	R/W	1	1: Off LED / LED Control by CS4227 0: Light LED
1	SFP2_LED_LINKACT_N	R/W	1	1: Off LED / LED Control by CS4227 0: Light LED
0	SFP1_LED_LINKACT_N	R/W	1	1: Off LED / LED Control by CS4227 0: Light LED

1.6. Line Card CPLD3 Register

Table 1-3 CPLD3 I/O Register Table

Address CPU	Register	R/W	Default value
0x01	CPLD version	Read Only	
0x08	QSFP Transceiver Reset-1	Read & Write	0xFF
0x09	QSFP Transceiver Reset-2	Read & Write	0xFF
0x0A	QSFP Transceiver Reset-3	Read & Write	0xFF
0x10	QSFP Transceiver Present-1	Read Only	
0x11	QSFP Transceiver Present-2	Read Only	
0x12	QSFP Transceiver Present-3	Read Only	
0x20	QSFP Transceiver Interrupt-1	Read Only	
0x21	QSFP Transceiver Interrupt-2	Read Only	
0x22	QSFP Transceiver Interrupt-3	Read Only	
0x30	System LED-1	Read & Write	0xFF
0x31	System LED-2	Read & Write	0xFF

1.6.1. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	0x00	CPLD version

1.6.2. Offset 0x08 QSFP Transceiver Reset-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	QSFP_RST_N_P28	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
6	QSFP_RST_N_P27	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
5	QSFP_RST_N_P26	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
4	QSFP_RST_N_P25	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
3	QSFP_RST_N_P24	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
2	QSFP_RST_N_P23	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

1	QSFP_RST_N_P22	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
0	QSFP_RST_N_P21	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

1.6.3. Offset 0x09 QSFP Transceiver Reset-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	QSFP_RST_N_P36	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
6	QSFP_RST_N_P35	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
5	QSFP_RST_N_P34	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
4	QSFP_RST_N_P33	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
3	QSFP_RST_N_P32	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
2	QSFP_RST_N_P31	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
1	QSFP_RST_N_P30	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
0	QSFP_RST_N_P29	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

1.6.4. Offset 0x0A QSFP Transceiver Reset-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	QSFP_RST_N_P40	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
2	QSFP_RST_N_P39	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
1	QSFP_RST_N_P38	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset

0	QSFP_RST_N_P37	R/W	1	1: Disable QSFP Transceiver Reset 0: Enable QSFP Transceiver Reset
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1.6.5. Offset 0x10 QSFP Transceiver Present-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_PRSNT_P28	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
6	QSFP_PRSNT_P27	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
5	QSFP_PRSNT_P26	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
4	QSFP_PRSNT_P25	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
3	QSFP_PRSNT_P24	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
2	QSFP_PRSNT_P23	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
1	QSFP_PRSNT_P22	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
0	QSFP_PRSNT_P21	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1.6.6. Offset 0x11 QSFP Transceiver Present-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_PRSNT_P36	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
6	QSFP_PRSNT_P35	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
5	QSFP_PRSNT_P34	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
4	QSFP_PRSNT_P33	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
3	QSFP_PRSNT_P32	R	NA	1: QSFP Transceiver did not present

				0: QSFP Transceiver is present
2	QSFP_PRSENT_P31	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
1	QSFP_PRSENT_P30	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
0	QSFP_PRSENT_P29	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1.6.7. Offset 0x12 QSFP Transceiver Present-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	QSFP_PRSENT_P40	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
2	QSFP_PRSENT_P39	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
1	QSFP_PRSENT_P38	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present
0	QSFP_PRSENT_P37	R	NA	1: QSFP Transceiver did not present 0: QSFP Transceiver is present

1.6.8. Offset 0x20 QSFP Transceiver Interrupt-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_INT_P28	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
6	QSFP_INT_P27	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
5	QSFP_INT_P26	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
4	QSFP_INT_P25	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
3	QSFP_INT_P24	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
2	QSFP_INT_P23	R	NA	1: QSFP Transceiver Interrupt de-assert

				0: QSFP Transceiver Interrupt assert
1	QSFP_INT_P22	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
0	QSFP_INT_P21	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert

1.6.9. Offset 0x21 QSFP Transceiver Interrupt-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP_INT_P36	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
6	QSFP_INT_P35	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
5	QSFP_INT_P34	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
4	QSFP_INT_P33	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
3	QSFP_INT_P32	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
2	QSFP_INT_P31	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
1	QSFP_INT_P30	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
0	QSFP_INT_P29	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert

1.6.10. Offset 0x22 QSFP Transceiver Interrupt-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:4	Reserve	NA	NA	
3	QSFP_INT_P40	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
2	QSFP_INT_P39	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert
1	QSFP_INT_P38	R	NA	1: QSFP Transceiver Interrupt de-assert

				0: QSFP Transceiver Interrupt assert
0	QSFP_INT_P37	R	NA	1: QSFP Transceiver Interrupt de-assert 0: QSFP Transceiver Interrupt assert

1.6.11. Offset 0x30 System LED-1 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	R/W	NA	
6	LOC_LED_B	R/W	1	1: Off LED 0: Light LED
5	LOC_LED_G	R/W	1	1: Off LED 0: Light LED
4	LOC_LED_R	R/W	1	1: Off LED 0: Light LED
3	Reserve	R/W	NA	
2	DIAG_LED_B	R/W	1	1: Off LED 0: Light LED
1	DIAG_LED_G	R/W	1	1: Off LED 0: Light LED
0	DIAG_LED_R	R/W	1	1: Off LED 0: Light LED

1.6.12. Offset 0x31 System LED-2 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	Reserve	R/W	NA	
6	FAN_LED_B	R/W	1	1: Off LED 0: Light LED
5	FAN_LED_G	R/W	1	1: Off LED 0: Light LED
4	FAN_LED_R	R/W	1	1: Off LED 0: Light LED
3	Reserve	R/W	NA	
2	PWR_LED_B	R/W	1	1: Off LED 0: Light LED

1	PWR_LED_G	R/W	1	1: Off LED 0: Light LED
0	PWR_LED_R	R/W	1	1: Off LED 0: Light LED

2. CPLD pin-out list

2.1. CPLD1 pin-out list

Table 2-1 CPLD1 Pin-out Table

Number	Net Name	Input/Output	Default Value
A10	RESET_MAC_N	Input	
A11	PCA9548_RESET_N	Output	
A12	GBX_SPI_RESET_N	Output	
A2	PSW_RST_L	Output	
A3	CS4227_EEPROM4	Output	
A4	SW1_SELECT	Output	
A5	J2_SYNCE_1_CLK_OUT_VALID	Input	
A6	UCD90320_RST_L	Output	Pull up
A7	EE_WP	Output	
A8	J2_PCIE_RST_N	Output	
A9	JITATT_INTERRUPT_N	Input	
B1	PSU2_PWOK_H	Input	
B10	JITATT_SPI_CS	Output	
B11	GBX10_INTR_N	Input	
B12	GBX9_INTR_N	Input	
B13	IDT33931_RST_N	Output	
B2	PSU2_PSON_L	Output	
B3	CS4227_RST_N	Output	
B4	J2_SYNCE_0_CLK_OUT_VALID	Input	
B5	CS4227_EEPROM3	Output	
B6	CS4227_EEPROM2	Output	
B7	JITATT_SPI_MISO	Input	
C1	PSU1_PWOK_H	Input	

C10	J2_INT_N	Input	
C11	CS4227_EEPROM1	Output	
C12	IDT33931_INT_REQ	Input	
C13	USB_RESET_N	Output	
C2	GBX_RCLK_SEC_SEL0	Output	
C9	J2_ROV1	Input	
D1	PSU1_SMB_ALERT_L	Input	
D11	LM75BD_SCLK	Input	
D12	LM75BD_CPLD_SDA_R	In/Output	
D13	CPLD2_INT_N	Input	
D6	PSU3_SMB_ALERT_L	Input	
D8	PSU4_SMB_ALERT_L	Input	
D9	HS_PWRGD	Input	
E1	PSU1_PRESENT_L	Input	
E10	CLK_SEL_4K	Output	
E12	GBX_RCLK_PRI_SEL1	Output	
E13	MAC_INT_L	Output	
E3	PSU2_PRESENT_L	Input	
E4	PSU3_PRESENT_L	Input	
E5	PSU2_SMB_ALERT_L	Input	
E6	CS4227_INT_N	Input	
E8	PCA9548_2_RESET_N	Output	
E9	IDT33931_DPLL1_LOCK	Input	
F1	PSU3_PWOK_H	Input	
F10	GBX_RESET_L	Output	
F12	GBX_RCLK_PRI_SEL0	Output	
F13	JITATT_I2C_SDA	In/Output	
F4	PSU4_PRESENT_L	Input	
F8	JITATT_LOCK	Input	
F9	UCD9090_ALERT_L	Input	
G10	JITATT_I2C_SCL	Output	
G12	CPLD23_RST	Output	
G13	PCB_VERSION0	Input	
G4	PSU1_PSON_L	Input	
G5	FRSYNC_CPLD_8K_1PPS	Input	

G9	PSW_INT_L	Input	
H1	RESET_SYS_CPLD_N	Input	
H10	MPHY_INT_N	Input	
H13	BOARD_ID0	Input	
H2	PSU3_PSON_L	Output	
H3	PSU4_PSON_L	Output	
H4	WANPLL_10M_CLK	Input	
H5	MFRSYNC_CPLD_2K_1PPS	Input	
H6	CPLD1_25MHZ	Input	
H8	HS_EN_CPLD	Output	Pull up
H9	BOARD_ID1	Input	
J1	I2C_1_SCL_CPLD1	Input	
J10	PCB_VERSION1	Input	
J12	CPLD3_INT_N	Input	
J13	MPHY_RESET_N	Output	
J2	STB_SDA_CPLD1	In/Output	
J5	GBX_RCLK_SEC_SEL2	Output	
J6	PSU_EEPROM_WP	Output	
J7	J2_ROV0	Input	
J8	GBX4_INTR_N	Input	
J9	HS_FAULT_N	Input	
K1	TJ2_TS0_TIME_VAL_R	Output	
K10	GBX7_INTR_N	Input	
K11	GBX8_INTR_N	Input	
K12	FAN_INT_L	Input	
K13	SYS_CPLD_INT_CPU	Output	
K2	J2_TOD_UART0_TX	Input	
K5	GBX_RCLK_SEC_SEL1	Output	
K6	LOWER_FAN_HS_PGD	Input	
K7	MANU_RST_N	Output	
K8	GBX5_INTR_N	Input	
L1	GBX_RCLK_SEC_SEL3	Output	
L10	J2_TOD_UART0_RX	Output	
L11	GBX3_INTR_N	Input	
L12	UCD90320_ALERT_L	Input	

L13	UCD90320_PON_RST_L	Input	
L2	J2_TS0_TIME_VAL_R	Output	
L3	GBX_RCLK_PRI_SEL3	Output	
L4	PSU4_PWOK_H	Input	
L5	PSU1_ACOK_H	Input	
M1	I2C_0_SCL_CPLD1	Input	
M10	GBX6_INTR_N	Input	
M11	GBX2_INTR_N	Input	
M12	OP2_GIO_L_R	Input	
M13	OP2_SRST_L_R	Output	
M2	SDA_CPLD1	In/Output	
M3	GBX_RCLK_PRI_SEL2	Output	
M4	PSU2_ACOK_H	Input	
M5	PSU3_ACOK_H	Input	
M7	J2_ROV2	Input	
M8	CPU_FAN_CPLD_RST_N	Output	
M9	UPPER_FAN_HS_PGD	Input	
N10	OP2_CRST_L_R	Output	
N11	CPU_PROCHOT	Input	
N12	OP2_PERST_L_R	Output	
N2	CPLD1_4K_CLK_R	Output	
N3	CPLD1_10M_CLK_R	Output	
N4	PSU4_ACOK_H	Input	
N5	IDT33931_DPLL3_LOCK	Input	
N6	IDT33931_DPLL2_LOCK	Input	
N7	MT25_RST_N	Output	
N8	J2_SYS_RST_N	Output	
N9	GBX1_INTR_N	Input	

2.2. CPLD2 LC pin-out list

Table 2-2 CPLD2 Pin-out Table

Number	Net Name	Input/Output	Default Value
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H5	CPLD2_25MHZ_OUT	Input	
N15	CPLD2_INT_N	Output	
H4	CPLD23_RST	Input	
J5	CPLD3_25MHZ_R	Output	
D3	I2C_0_SCL_CPLD2	Input	
C2	J2_LED_CLK0	Input	
D1	J2_LED_CLK1	Input	
C3	J2_LED_DATA0	Input	
D2	J2_LED_DATA1	Input	
T5	PRESENT_FX0	Input	
T8	PRESENT_FX1	Input	
G12	QSFP_INT_P01	Input	
G13	QSFP_INT_P02	Input	
M16	QSFP_INT_P03	Input	
A8	QSFP_INT_P04	Input	
C5	QSFP_INT_P05	Input	
D8	QSFP_INT_P06	Input	
B3	QSFP_INT_P07	Input	
A4	QSFP_INT_P08	Input	
K3	QSFP_INT_P09	Input	
F6	QSFP_INT_P10	Input	
N2	QSFP_INT_P11	Input	
M2	QSFP_INT_P12	Input	
N9	QSFP_INT_P13	Input	
P4	QSFP_INT_P14	Input	
T11	QSFP_INT_P15	Input	
T10	QSFP_INT_P16	Input	
J13	QSFP_INT_P17	Input	
P12	QSFP_INT_P18	Input	
K15	QSFP_INT_P19	Input	
K16	QSFP_INT_P20	Input	
C14	QSFP_LK_LED_B_01	Output	
C10	QSFP_LK_LED_B_02	Output	
G15	QSFP_LK_LED_B_03	Output	
C15	QSFP_LK_LED_B_04	Output	

A12	QSFP_LK_LED_B_05	Output	
E10	QSFP_LK_LED_B_06	Output	
C13	QSFP_LK_LED_B_07	Output	
D7	QSFP_LK_LED_B_08	Output	
F1	QSFP_LK_LED_B_09	Output	
E7	QSFP_LK_LED_B_10	Output	
F4	QSFP_LK_LED_B_11	Output	
J4	QSFP_LK_LED_B_12	Output	
P7	QSFP_LK_LED_B_13	Output	
K2	QSFP_LK_LED_B_14	Output	
R5	QSFP_LK_LED_B_15	Output	
N8	QSFP_LK_LED_B_16	Output	
N12	QSFP_LK_LED_B_17	Output	
M11	QSFP_LK_LED_B_18	Output	
M13	QSFP_LK_LED_B_19	Output	
J14	QSFP_LK_LED_B_20	Output	
D12	QSFP_LK_LED_G_01	Output	
D9	QSFP_LK_LED_G_02	Output	
G16	QSFP_LK_LED_G_03	Output	
D15	QSFP_LK_LED_G_04	Output	
B12	QSFP_LK_LED_G_05	Output	
A11	QSFP_LK_LED_G_06	Output	
F12	QSFP_LK_LED_G_07	Output	
C7	QSFP_LK_LED_G_08	Output	
F2	QSFP_LK_LED_G_09	Output	
E6	QSFP_LK_LED_G_10	Output	
F3	QSFP_LK_LED_G_11	Output	
H1	QSFP_LK_LED_G_12	Output	
N7	QSFP_LK_LED_G_13	Output	
L1	QSFP_LK_LED_G_14	Output	
R4	QSFP_LK_LED_G_15	Output	
R8	QSFP_LK_LED_G_16	Output	
N13	QSFP_LK_LED_G_17	Output	
P11	QSFP_LK_LED_G_18	Output	
N14	QSFP_LK_LED_G_19	Output	

K13	QSFP_LK_LED_G_20	Output	
D14	QSFP_LK_LED_R_01	Output	
D10	QSFP_LK_LED_R_02	Output	
F16	QSFP_LK_LED_R_03	Output	
D16	QSFP_LK_LED_R_04	Output	
B11	QSFP_LK_LED_R_05	Output	
E11	QSFP_LK_LED_R_06	Output	
F11	QSFP_LK_LED_R_07	Output	
B7	QSFP_LK_LED_R_08	Output	
H3	QSFP_LK_LED_R_09	Output	
A2	QSFP_LK_LED_R_10	Output	
E3	QSFP_LK_LED_R_11	Output	
H2	QSFP_LK_LED_R_12	Output	
N6	QSFP_LK_LED_R_13	Output	
K1	QSFP_LK_LED_R_14	Output	
R1	QSFP_LK_LED_R_15	Output	
P8	QSFP_LK_LED_R_16	Output	
P14	QSFP_LK_LED_R_17	Output	
M10	QSFP_LK_LED_R_18	Output	
R14	QSFP_LK_LED_R_19	Output	
K14	QSFP_LK_LED_R_20	Output	
G14	QSFP_PRSNT_P01	Input	
H13	QSFP_PRSNT_P02	Input	
A9	QSFP_PRSNT_P03	Input	
C9	QSFP_PRSNT_P04	Input	
D6	QSFP_PRSNT_P05	Input	
C8	QSFP_PRSNT_P06	Input	
B4	QSFP_PRSNT_P07	Input	
B5	QSFP_PRSNT_P08	Input	
L4	QSFP_PRSNT_P09	Input	
D4	QSFP_PRSNT_P10	Input	
M4	QSFP_PRSNT_P11	Input	
M3	QSFP_PRSNT_P12	Input	
M9	QSFP_PRSNT_P13	Input	
N3	QSFP_PRSNT_P14	Input	



R10	QSFP_PRSNT_P15	Input	
P10	QSFP_PRSNT_P16	Input	
M12	QSFP_PRSNT_P17	Input	
R12	QSFP_PRSNT_P18	Input	
L16	QSFP_PRSNT_P19	Input	
J15	QSFP_PRSNT_P20	Input	
H14	QSFP_RST_N_P01	Output	
F14	QSFP_RST_N_P02	Output	
F13	QSFP_RST_N_P03	Output	
B8	QSFP_RST_N_P04	Output	
E8	QSFP_RST_N_P05	Output	
A6	QSFP_RST_N_P06	Output	
D5	QSFP_RST_N_P07	Output	
B1	QSFP_RST_N_P08	Output	
F5	QSFP_RST_N_P09	Output	
K4	QSFP_RST_N_P10	Output	
L3	QSFP_RST_N_P11	Output	
P2	QSFP_RST_N_P12	Output	
R3	QSFP_RST_N_P13	Output	
R7	QSFP_RST_N_P14	Output	
N10	QSFP_RST_N_P15	Output	
R11	QSFP_RST_N_P16	Output	
T15	QSFP_RST_N_P17	Output	
N11	QSFP_RST_N_P18	Output	
J16	QSFP_RST_N_P19	Output	
L15	QSFP_RST_N_P20	Output	
E13	QSFP_SP_LED_B_01	Output	
C11	QSFP_SP_LED_B_02	Output	
E16	QSFP_SP_LED_B_03	Output	
H15	QSFP_SP_LED_B_04	Output	
A15	QSFP_SP_LED_B_05	Output	
B13	QSFP_SP_LED_B_06	Output	
A10	QSFP_SP_LED_B_07	Output	
A7	QSFP_SP_LED_B_08	Output	
G4	QSFP_SP_LED_B_09	Output	

K5	QSFP_SP_LED_B_10	Output	
E4	QSFP_SP_LED_B_11	Output	
G1	QSFP_SP_LED_B_12	Output	
L5	QSFP_SP_LED_B_13	Output	
J1	QSFP_SP_LED_B_14	Output	
M1	QSFP_SP_LED_B_15	Output	
M7	QSFP_SP_LED_B_16	Output	
T13	QSFP_SP_LED_B_17	Output	
L12	QSFP_SP_LED_B_18	Output	
R16	QSFP_SP_LED_B_19	Output	
L14	QSFP_SP_LED_B_20	Output	
D13	QSFP_SP_LED_G_01	Output	
C12	QSFP_SP_LED_G_02	Output	
F15	QSFP_SP_LED_G_03	Output	
E15	QSFP_SP_LED_G_04	Output	
B14	QSFP_SP_LED_G_05	Output	
E12	QSFP_SP_LED_G_06	Output	
E9	QSFP_SP_LED_G_07	Output	
B6	QSFP_SP_LED_G_08	Output	
G3	QSFP_SP_LED_G_09	Output	
C6	QSFP_SP_LED_G_10	Output	
E2	QSFP_SP_LED_G_11	Output	
M15	QSFP_SP_LED_G_12	Output	
P6	QSFP_SP_LED_G_13	Output	
J2	QSFP_SP_LED_G_14	Output	
N1	QSFP_SP_LED_G_15	Output	
P5	QSFP_SP_LED_G_16	Output	
R13	QSFP_SP_LED_G_17	Output	
L11	QSFP_SP_LED_G_18	Output	
P15	QSFP_SP_LED_G_19	Output	
M14	QSFP_SP_LED_G_20	Output	
E14	QSFP_SP_LED_R_01	Output	
D11	QSFP_SP_LED_R_02	Output	
B9	QSFP_SP_LED_R_03	Output	
H16	QSFP_SP_LED_R_04	Output	

B16	QSFP_SP_LED_R_05	Output	
A13	QSFP_SP_LED_R_06	Output	
B10	QSFP_SP_LED_R_07	Output	
A5	QSFP_SP_LED_R_08	Output	
C4	QSFP_SP_LED_R_09	Output	
G2	QSFP_SP_LED_R_10	Output	
E5	QSFP_SP_LED_R_11	Output	
N16	QSFP_SP_LED_R_12	Output	
N5	QSFP_SP_LED_R_13	Output	
J3	QSFP_SP_LED_R_14	Output	
L2	QSFP_SP_LED_R_15	Output	
M6	QSFP_SP_LED_R_16	Output	
T12	QSFP_SP_LED_R_17	Output	
K12	QSFP_SP_LED_R_18	Output	
P13	QSFP_SP_LED_R_19	Output	
L13	QSFP_SP_LED_R_20	Output	
R6	RX_LOSS_FX0	Input	
T2	RX_LOSS_FX1	Input	
E1	SDA_CPLD2	In/Output	
T9	SFP1_LED_ERR_N	Output	
R9	SFP1_LED_LINKACT_N	Output	
M8	SFP2_LED_ERR_N	Output	
P9	SFP2_LED_LINKACT_N	Output	
T4	TX_DIS_FX0	Output	
T7	TX_DIS_FX1	Output	

2.3. CPLD3 LC pin-out list

Table 2-3 CPLD3 Pin-out Table

Number	Net Name	Input/Output	Default Value
C6	CPLD23_RST	Input	
H5	CPLD3_25MHZ	Input	
L5	CPLD3_INT_N	Output	
N2	DIAG_LED_B	Output	

M1	DIAG_LED_G	Output	
N1	DIAG_LED_R	Output	
M3	FAN_LED_B	Output	
M4	FAN_LED_G	Output	
M8	FAN_LED_R	Output	
A15	I2C_0_SCL_CPLD3	Input	
A10	J2_LED_CLK2	Input	
A12	J2_LED_CLK3	Input	
A11	J2_LED_DATA2	Input	
A13	J2_LED_DATA3	Input	
P2	LOC_LED_B	Output	
N3	LOC_LED_G	Output	
M2	LOC_LED_R	Output	
J12	PWR_LED_B	Output	
H12	PWR_LED_G	Output	
M9	PWR_LED_R	Output	
D7	QSFP_INT_P21	Input	
A8	QSFP_INT_P22	Input	
D4	QSFP_INT_P23	Input	
A4	QSFP_INT_P24	Input	
G2	QSFP_INT_P25	Input	
F1	QSFP_INT_P26	Input	
K2	QSFP_INT_P27	Input	
H1	QSFP_INT_P28	Input	
T4	QSFP_INT_P29	Input	
L2	QSFP_INT_P30	Input	
P6	QSFP_INT_P31	Input	
P5	QSFP_INT_P32	Input	
P11	QSFP_INT_P33	Input	
N8	QSFP_INT_P34	Input	
M14	QSFP_INT_P35	Input	
N14	QSFP_INT_P36	Input	
F11	QSFP_INT_P37	Input	
G16	QSFP_INT_P38	Input	
C13	QSFP_INT_P39	Input	

B16	QSFP_INT_P40	Input	
C11	QSFP_LK_LED_B_21	Output	
C4	QSFP_LK_LED_B_22	Output	
B8	QSFP_LK_LED_B_23	Output	
E10	QSFP_LK_LED_B_24	Output	
F6	QSFP_LK_LED_B_25	Output	
F5	QSFP_LK_LED_B_26	Output	
M7	QSFP_LK_LED_B_27	Output	
L3	QSFP_LK_LED_B_28	Output	
R1	QSFP_LK_LED_B_29	Output	
M10	QSFP_LK_LED_B_30	Output	
R11	QSFP_LK_LED_B_31	Output	
R14	QSFP_LK_LED_B_32	Output	
J13	QSFP_LK_LED_B_33	Output	
H13	QSFP_LK_LED_B_34	Output	
L16	QSFP_LK_LED_B_35	Output	
P13	QSFP_LK_LED_B_36	Output	
H14	QSFP_LK_LED_B_37	Output	
F13	QSFP_LK_LED_B_38	Output	
D16	QSFP_LK_LED_B_39	Output	
D12	QSFP_LK_LED_B_40	Output	
D10	QSFP_LK_LED_G_21	Output	
B13	QSFP_LK_LED_G_22	Output	
A9	QSFP_LK_LED_G_23	Output	
E9	QSFP_LK_LED_G_24	Output	
E8	QSFP_LK_LED_G_25	Output	
F4	QSFP_LK_LED_G_26	Output	
M11	QSFP_LK_LED_G_27	Output	
K4	QSFP_LK_LED_G_28	Output	
C2	QSFP_LK_LED_G_29	Output	
P10	QSFP_LK_LED_G_30	Output	
N10	QSFP_LK_LED_G_31	Output	
R13	QSFP_LK_LED_G_32	Output	
K12	QSFP_LK_LED_G_33	Output	
J15	QSFP_LK_LED_G_34	Output	

L15	QSFP_LK_LED_G_35	Output	
P12	QSFP_LK_LED_G_36	Output	
H16	QSFP_LK_LED_G_37	Output	
F14	QSFP_LK_LED_G_38	Output	
D15	QSFP_LK_LED_G_39	Output	
E11	QSFP_LK_LED_G_40	Output	
D11	QSFP_LK_LED_R_21	Output	
B4	QSFP_LK_LED_R_22	Output	
B9	QSFP_LK_LED_R_23	Output	
C9	QSFP_LK_LED_R_24	Output	
E6	QSFP_LK_LED_R_25	Output	
E3	QSFP_LK_LED_R_26	Output	
L11	QSFP_LK_LED_R_27	Output	
K3	QSFP_LK_LED_R_28	Output	
L1	QSFP_LK_LED_R_29	Output	
R7	QSFP_LK_LED_R_30	Output	
T5	QSFP_LK_LED_R_31	Output	
T13	QSFP_LK_LED_R_32	Output	
L12	QSFP_LK_LED_R_33	Output	
J14	QSFP_LK_LED_R_34	Output	
M16	QSFP_LK_LED_R_35	Output	
T12	QSFP_LK_LED_R_36	Output	
H15	QSFP_LK_LED_R_37	Output	
G13	QSFP_LK_LED_R_38	Output	
D13	QSFP_LK_LED_R_39	Output	
B14	QSFP_LK_LED_R_40	Output	
C7	QSFP_PRSNT_P21	Input	
C8	QSFP_PRSNT_P22	Input	
D3	QSFP_PRSNT_P23	Input	
B5	QSFP_PRSNT_P24	Input	
G1	QSFP_PRSNT_P25	Input	
D2	QSFP_PRSNT_P26	Input	
H2	QSFP_PRSNT_P27	Input	
G3	QSFP_PRSNT_P28	Input	
T2	QSFP_PRSNT_P29	Input	

J1	QSFP_PRSNT_P30	Input	
N6	QSFP_PRSNT_P31	Input	
R4	QSFP_PRSNT_P32	Input	
T9	QSFP_PRSNT_P33	Input	
T8	QSFP_PRSNT_P34	Input	
M13	QSFP_PRSNT_P35	Input	
R16	QSFP_PRSNT_P36	Input	
F12	QSFP_PRSNT_P37	Input	
K13	QSFP_PRSNT_P38	Input	
C15	QSFP_PRSNT_P39	Input	
F16	QSFP_PRSNT_P40	Input	
A6	QSFP_RST_N_P21	Output	
B6	QSFP_RST_N_P22	Output	
C5	QSFP_RST_N_P23	Output	
E4	QSFP_RST_N_P24	Output	
F2	QSFP_RST_N_P25	Output	
E2	QSFP_RST_N_P26	Output	
F3	QSFP_RST_N_P27	Output	
K1	QSFP_RST_N_P28	Output	
D1	QSFP_RST_N_P29	Output	
R3	QSFP_RST_N_P30	Output	
P4	QSFP_RST_N_P31	Output	
T7	QSFP_RST_N_P32	Output	
R8	QSFP_RST_N_P33	Output	
T10	QSFP_RST_N_P34	Output	
P15	QSFP_RST_N_P35	Output	
L13	QSFP_RST_N_P36	Output	
L14	QSFP_RST_N_P37	Output	
G15	QSFP_RST_N_P38	Output	
F15	QSFP_RST_N_P39	Output	
C14	QSFP_RST_N_P40	Output	
B7	QSFP_SP_LED_B_21	Output	
D6	QSFP_SP_LED_B_22	Output	
B10	QSFP_SP_LED_B_23	Output	
B3	QSFP_SP_LED_B_24	Output	

D8	QSFP_SP_LED_B_25	Output	
E5	QSFP_SP_LED_B_26	Output	
H4	QSFP_SP_LED_B_27	Output	
J4	QSFP_SP_LED_B_28	Output	
L4	QSFP_SP_LED_B_29	Output	
N7	QSFP_SP_LED_B_30	Output	
R5	QSFP_SP_LED_B_31	Output	
N12	QSFP_SP_LED_B_32	Output	
P8	QSFP_SP_LED_B_33	Output	
P9	QSFP_SP_LED_B_34	Output	
N16	QSFP_SP_LED_B_35	Output	
T11	QSFP_SP_LED_B_36	Output	
J16	QSFP_SP_LED_B_37	Output	
K14	QSFP_SP_LED_B_38	Output	
E13	QSFP_SP_LED_B_39	Output	
E12	QSFP_SP_LED_B_40	Output	
C12	QSFP_SP_LED_G_21	Output	
A5	QSFP_SP_LED_G_22	Output	
C10	QSFP_SP_LED_G_23	Output	
D9	QSFP_SP_LED_G_24	Output	
E7	QSFP_SP_LED_G_25	Output	
E1	QSFP_SP_LED_G_26	Output	
H3	QSFP_SP_LED_G_27	Output	
K5	QSFP_SP_LED_G_28	Output	
M6	QSFP_SP_LED_G_29	Output	
P7	QSFP_SP_LED_G_30	Output	
R6	QSFP_SP_LED_G_31	Output	
N11	QSFP_SP_LED_G_32	Output	
M12	QSFP_SP_LED_G_33	Output	
R9	QSFP_SP_LED_G_34	Output	
M15	QSFP_SP_LED_G_35	Output	
N13	QSFP_SP_LED_G_36	Output	
K15	QSFP_SP_LED_G_37	Output	
G14	QSFP_SP_LED_G_38	Output	
D14	QSFP_SP_LED_G_39	Output	

E16	QSFP_SP_LED_G_40	Output	
A7	QSFP_SP_LED_R_21	Output	
B12	QSFP_SP_LED_R_22	Output	
B11	QSFP_SP_LED_R_23	Output	
C3	QSFP_SP_LED_R_24	Output	
B1	QSFP_SP_LED_R_25	Output	
D5	QSFP_SP_LED_R_26	Output	
G4	QSFP_SP_LED_R_27	Output	
J3	QSFP_SP_LED_R_28	Output	
J2	QSFP_SP_LED_R_29	Output	
N5	QSFP_SP_LED_R_30	Output	
R10	QSFP_SP_LED_R_31	Output	
R12	QSFP_SP_LED_R_32	Output	
T15	QSFP_SP_LED_R_33	Output	
N9	QSFP_SP_LED_R_34	Output	
N15	QSFP_SP_LED_R_35	Output	
P14	QSFP_SP_LED_R_36	Output	
K16	QSFP_SP_LED_R_37	Output	
G12	QSFP_SP_LED_R_38	Output	
E14	QSFP_SP_LED_R_39	Output	
E15	QSFP_SP_LED_R_40	Output	
A2	SDA_CPLD3	In/Output	